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L1: Entry 1 of 2

File: JPAB

Sep 27, 2002

PUB-NO: JP02002280391A

DOCUMENT-IDENTIFIER: JP 2002280391 A

TITLE: SEMICONDUCTOR DEVICE USING SELF-ALIGNED CRYSTALLIZATION BY METAL INDUCTION IN SILICON LAYER FOR TFTS, TOP-GATE TYPE TFT AND TOP-GATE TYPE TFT MANUFACTURING METHOD

PUBN-DATE: September 27, 2002

## INVENTOR- INFORMATION:

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## ASSIGNEE- INFORMATION:

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INTERNATL BUSINESS MACH CORP	

APPL-NO: JP2002008478

APPL-DATE: January 17, 2002

PRIORITY-DATA: 2001US-765134 (January 18, 2001)

INT-CL (IPC): H01 L 21/336; G02 F 1/1362; G02 F 1/1368; H01 L 21/20; H01 L 29/786

## ABSTRACT:

PROBLEM TO BE SOLVED: To provide a semiconductor device, a thin-film transistor (TFT) and TFT manufacturing method.

SOLUTION: The semiconductor device includes a top-gate type thin-film transistor (TFT) which is formed on a substrate 1. The top-gate type TFT comprises an insulation layer 3 deposited on the substrate 1, a source and drain electrodes 4, 5 of a metal - dopant compound deposited on the insulation layer 3, a polycrystalline Si(poly-Si) layer 6 deposited on the upsides of the insulation layer 3, the source and drain electrodes 4, 5, an Ohmic contact layer 7, formed by migration of the dopant from the metal - dopant compound between the metal - dopant compound and the poly-Si layer 6, a gate insulation layer 9 deposited on the poly-Si layer 6 and a gate electrode 10 formed on the gate insulation layer 9. The poly-Si layer 6 is crystallized by lateral crystallization due to the metal induction.

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L3: Entry 2 of 15

File: JPAB

Sep 27, 2002

PUB-NO: JP02002280391A

DOCUMENT-IDENTIFIER: JP 2002280391 A

TITLE: SEMICONDUCTOR DEVICE USING SELF-ALIGNED CRYSTALLIZATION BY METAL INDUCTION IN SILICON LAYER FOR TFTS, TOP-GATE TYPE TFT AND TOP-GATE TYPE TFT MANUFACTURING METHOD

PUBN-DATE: September 27, 2002

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